Page #	Frame #	Valid
0x0	0x00234	1
0x1	0x00235	1
0x2	0x0023f	1
0x3	0x00ace	1
0x4	0x00004	1

Consider a paging-based virtual memory system with 32-bit virtual and physical adresses, and a page size of 2^{12} bytes (4 KiB). Suppose that a process P is running. P uses only 128 KiB of virtual memory. The first 5 entries of P's page table are shown below.

Question 1. What is the total number of entries in P's page table?

Question 2. How many entries are valid?

Question 3. What physical addresses correspond to each of these virtual addresses?

- 0x00001a60
- 0x00000fb5
- 0x00004664

Question 4. How many bits of the address correspond to the page offset and to the virtual page number?

Question 5. If each page table level in a radix-tree is page sized. How many bits would be used to index each level of the radix-tree and how many levels will you need to describe the entire address space?

Question 6. If the page size were 16 KiB instead of 4 KiB, how many entries would there be in P's page table? How many bits of each virtual address would be used for the offset, and how many for the page number?