CS350 Operating Systems

In-Class Problems: Multi-Level Paging

Consider a virtual memory system that uses multi-level paging for address translation. Virtual addresses and physical addresses are 64 bits long. The page size is 1 MB (2^{20} bytes). The size of a page table entry is 16 (2^4) bytes. Each individual page table, at each level, must fit in a single frame.

Q1: How many bits of each virtual address are needed to represent the page offset?

Q2: What is the maximum number of entries in an individual page table?

Q3: What is the number of levels of page tables that will be required for virtual-to-physical translation in this system?

Q4: Suppose that a particular process uses only 128 MB (2^{27} bytes) of virtual memory, with a virtual address range from 0 to $2^{27} - 1$. How many individual page tables, *at each level*, will be required to translate this process' address space?