Chapter 1

Complete I/O Port List

Here is some public domain information on I/O Ports. Many of the devices mentioned here are not installed on the Eos systems. Other devices (like the floppy) are probably not of interest. Information on EISA systems has been removed since Eos systems do not have an EISA bus (instead, they have PCI).

The original authors give us this warning:

> Do *not* consider this information as complete and accurate. If you want to do hardware programming check *always* the appropriate data sheets. Be aware that erroneously programming can put your hardware or your data at risk.

Some terminalogy used here is different than in the rest of this documentation. In particular, these authors use PIC (Programable Interrupt Controller) to refer to what the rest of this documents calls the ICU (Interrupt Control Unit). When in doubt, the chip numbers are the best name and you should be encouraged to use the chip numbers because it makes you sound really knowledgable.

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0000-001F ----  DMA 1   (first Direct Memory Access controller 8237)

0000    r/w     DMA channel 0  address  byte  0, then byte 1.
0001    r/w     DMA channel 0 word count byte 0, then byte 1.
0002    r/w     DMA channel 1  address  byte  0, then byte 1.
0003    r/w     DMA channel 1 word count byte 0, then byte 1.
0004    r/w     DMA channel 2  address  byte  0, then byte 1.
0005    r/w     DMA channel 2 word count byte 0, then byte 1.
0006    r/w     DMA channel 3  address  byte  0, then byte 1.
0007    r/w     DMA channel 3 word count byte 0, then byte 1.

0008    r       DMA channel 0-3 status register
                 bit 7 = 1  channel 3 request
                 bit 6 = 1  channel 2 request
                 bit 5 = 1  channel 1 request
                 bit 4 = 1  channel 0 request
                 bit 3 = 1  channel terminal count on channel 3
                 bit 2 = 1  channel terminal count on channel 2
                 bit 1 = 1  channel terminal count on channel 1
                 bit 0 = 1  channel terminal count on channel 0

0008    w       DMA channel 0-3 command register
                 bit 7 = 1  DACK sense active high
                       = 0  DACK sense active low
                 bit 6 = 1  DREQ sense active high
                       = 0  DREQ sense active low
                 bit 5 = 1  extended write selection
                       = 0  late write selection
                 bit 4 = 1  rotating priority
                       = 0  fixed priority
                 bit 3 = 1  compressed timing
                       = 0  normal timing
                 bit 2 = 1  enable controller
                       = 0  enable memory-to-memory

0009    w       DMA write request register

000A    r/w     DMA channel 0-3 mask register
                 bit 7-3 = 0   reserved
                 bit 2   = 0   clear mask bit
                         = 1   set mask bit
                 bit 1-0 = 00  channel 0 select
                         = 01  channel 1 select
                         = 10  channel 2 select
                         = 11  channel 3 select

000B    w       DMA channel 0-3 mode register
                 bit 7-6 = 00  demand mode
                         = 01  single mode
                         = 10  block mode
                         = 11  cascade mode
                 bit 5   = 0   address increment select
                         = 1   address decrement select
                 bit 3-2 = 00  verify operation
                         = 01  write to memory
                         = 10  read from memory
                         = 11  reserved
                 bit 1-0 = 00  channel 0 select
                         = 01  channel 1 select
                         = 10  channel 2 select
                         = 11  channel 3 select

000C    w       DMA clear byte pointer flip-flop
000D    r       DMA read temporary register
000D    w       DMA master clear
000E    w       DMA clear mask register
000F    w       DMA write mask register

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0020-003F ----  PIC 1   (Programmable Interrupt Controller 8259)

0020    w       PIC initialization command word ICW1
                 bit 7-5 = 0  only used in 80/85 mode
                 bit 4   = 1  ICW1 is being issued
                 bit 3   = 0  edge triggered mode
                         = 1  level triggered mode
                 bit 2   = 0  successive interrupt vectors use 8 bytes
                         = 1  successive interrupt vectors use 4 bytes
                 bit 1   = 0  cascade mode
                         = 1  single mode, no ICW3 needed
                 bit 0   = 0  no ICW4 needed
                         = 1  ICW4 needed

0021    w       PIC  ICW2,ICW3,ICW4 after ICW1 to 0020
                ICW2:
                 bit 7-3 = address lines A0-A3 of base vector address for PIC
                 bit 2-0 = reserved
                ICW3:
                 bit 7-0 = 0  slave controller not attached to corresponding
                              interrupt pin
                         = 1  slave controller attached to corresponding
                              interrupt pin
                ICW4:
                 bit 7-5 = 0  reserved
                 bit 4   = 0  no special fully-nested mode
                         = 1  special fully-nested mode
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		 bit 3-2 = 0x nonbuffered mode
			 = 10 buffered mode/slave
			 = 11 buffered mode/master
		 bit 1	 = 0  normal EOI
			 = 1  Auto EOI
		 bit 0	 = 0  8085 mode
			 = 1  8086/8088 mode

0021	r/w	PIC master interrupt mask register
		OCW1:
		 bit 7 = 0  enable parallel printer interrupt
		 bit 6 = 0  enable diskette interrupt
		 bit 5 = 0  enable fixed disk interrupt
		 bit 4 = 0  enable serial port 1 interrupt
		 bit 3 = 0  enable serial port 2 interrupt
		 bit 2 = 0  enable video interrupt
		 bit 1 = 0  enable keyboard, mouse, RTC interrupt
		 bit 0 = 0  enable timer interrupt

0020	r	PIC  interrupt request/in-service registers by OCW3
		request register:
		 bit 7-0 = 0  no active request for the corresponding int. line
			 = 1  active request for corresponding interrupt line
		in-service register:
		 bit 7-0 = 0  corresponding line not currently being serviced
			 = 1  corresponding int. line currently being serviced

0020	w	OCW2:
		 bit 7-5 = 000	rotate in auto EOI mode (clear)
			 = 001	nonspecific EOI
			 = 010	no operation
			 = 011	specific EOI
			 = 100	rotate in auto EOI mode (set)
			 = 101	rotate on nonspecific EOI command
			 = 110	set priority command
			 = 111	rotate on specific EOI command
		 bit 4	 = 0	reserved
		 bit 3	 = 0	reserved
		 bit 2-0	interrupt request to which the command applies

0020	w	PIC OCW3
		 bit 7	 = 0   reserved
		 bit 6-5 = 0x  no operation
			 = 10  reset special mask
			 = 11  set special mask
		 bit 4	 = 0   reserved
		 bit 3	 = 1   reserved
		 bit 2	 = 0   no poll command
			 = 1   poll command
		 bit 1-0 = 0x  no operation
			 = 10  read int.request register on next read at 0020
			 = 11  read int.in-service register on next read 0020

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0022-002B ----	Intel 82355, part of chipset for 386sx
		 initialisation in POST will disable these addresses,
		 only a hard reset will enable them again.

0022	r/w	82335 MCR memory configuration register
0024		82335 RC1 roll compare register
0026		82335 RC2 roll compare register
0028		82335 CC0 compare register
002A		82335 CC1 compare register

		  values for CC0 and CC1:
		  00F9,0000  enable range compare CC0 0-512K  CC1 disable
		  00F1,0000  enable range compare CC0 0-1024K CC1 disable
		  00F1,10F9  enable range compare CC0 0-1M    CC1 1M-1M5
		  00E1,0000  enable range compare CC0 0-2M    CC1 disable
		  00E1,0000  enable range compare CC0 0-2M    CC1 disable
		  00C1,0000  enable range compare CC0 0-4M    CC1 disable
		  00C1,40E1  enable range compare CC0 0-4M    CC1 4M-6M
		  0081,0000  enable range compare CC0 0-8M    CC1 disable

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0022-0023 ----	Chip Set Data

0022	w	index for accesses to data port
0023	r/w	chip set data

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0022-0023 ----	Cyrix Cx486SLC/DLC processor Cache Configuration Registers

0022	w	index for accesses to next port
		C0h CR0
		C1h CR1
		C4h non-cacheable region 1, start address bits 31-24
		C5h non-cacheable region 1, start address bits 23-16
		C6h non-cacheable region 1, start addr 15-12, size (low nibble)
		C7h non-cacheable region 2, start address bits 31-24
		C8h non-cacheable region 2, start address bits 23-16
		C9h non-cacheable region 2, start addr 15-12, size (low nibble)
		CAh non-cacheable region 3, start address bits 31-24
		CBh non-cacheable region 3, start address bits 23-16
		CCh non-cacheable region 3, start addr 15-12, size (low nibble)
		CDh non-cacheable region 4, start address bits 31-24
		CEh non-cacheable region 4, start address bits 23-16
		CFh non-cacheable region 4, start addr 15-12, size (low nibble)
0023	r/w	cache configuration register array (indexed by port 0022h)

		non-cacheable region sizes:
		 00h  disabled
		 01h  4K
		 02h  8K
		 03h  16K
		 04h  32K
		 05h  64K
		 06h  128K
		 07h  256K
		 08h  512K
		 09h  1M
		 0Ah  2M
		 0Bh  4M
		 0Ch  8M
		 0Dh  16M
		 0Eh  32M
		 0Fh  4G

		Configuration Register 0 format:
		 bit 0	"NC0" first 64K of each 1M noncacheable in real/V86
		 bit 1	"NC1" 640K-1M noncacheable
		 bit 2	"A20M" enables A20M# input pin
		 bit 3	"KEN"  enables KEN# input pin
		 bit 4	"FLUSH" enables KEN# input pin
		 bit 5	"BARB" enables internal cache flushing on bus holds
		 bit 6	"C0" cache direct-mapped instead of 2-way associative
		 bit 7	"SUSPEND" enables SUSP# input and SUSPA# output pins

		Configuration Register 1 format;
		 bit 0	"RPL" enables output pins RPLSET and RPLVAL#

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0026-0027 ----	Power Management

0026	w	index for data port
0027	r/w	power management data

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0040-005F ----	PIT  (Programmable Interrupt Timer  8253, 8254)
		 XT & AT uses 40-43    PS/2 uses 40, 42,43,44, 47

0040	r/w	PIT  counter 0, counter divisor       (XT, AT, PS/2)
0041	r/w	PIT  counter 1, RAM refresh counter   (XT, AT)
0042	r/w	PIT  counter 2, cassette & speaker    (XT, AT, PS/2)

0043	r/w	PIT  mode port, control word register for counters 0-2
		 bit 7-6 = 00  counter 0 select
			 = 01  counter 1 select   (not PS/2)
			 = 10  counter 2 select
		 bit 5-4 = 00  counter latch command
			 = 01  read/write counter bits 0-7 only
			 = 10  read/write counter bits 8-15 only
			 = 11  read/write counter bits 0-7 first, then 8-15
		 bit 3-1 = 000 mode 0 select
			 = 001 mode 1 select - programmable one shot
			 = x10 mode 2 select - rate generator
			 = x11 mode 3 select - square wave generator
			 = 100 mode 4 select - software triggered strobe
			 = 101 mode 5 select - hardware triggered strobe
		 bit 0	 = 0   binary counter 16 bits
			 = 1   BCD counter

0044	r/w	PIT  counter 3 (PS/2, EISA)
		used as fail-safe timer. generates an NMI on time out.
		for user generated NMI see at 0462.

0047	w	PIT  control word register counter 3 (PS/2, EISA)
		 bit 7-6 = 00  counter 3 select
			 = 01  reserved
			 = 10  reserved
			 = 11  reserved
		 bit 5-4 = 00  counter latch command counter 3
			 = 01  read/write counter bits 0-7 only
			 = 1x  reserved
		 bit 3-0 = 00

0048		EISA
0049		8254 timer 2, not used (counter 1)
004A		EISA programmable interval timer 2
004B		EISA programmable interval timer 2

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0060-006F ----	Keyboard controller 804x (8041, 8042)  (or PPI (8255) on PC,XT)
		 XT uses 60-63,  AT uses 60-64

		 AT keyboard controller input port bit definitions
		  bit 7	  = 0  keyboard inhibited
		  bit 6	  = 0  CGA, else MDA
		  bit 5	  = 0  manufacturing jumper installed
		  bit 4	  = 0  system RAM 512K, else 640K
		  bit 3-0      reserved

		 AT keyboard controller input port bit definitions by Compaq
		  bit 7	  = 0  security lock is locked
		  bit 6	  = 0  Compaq dual-scan display, 1=non-Compaq display
		  bit 5	  = 0  system board dip switch 5 is ON
		  bit 4	  = 0  auto speed selected, 1=high speed selected
		  bit 3	  = 0  slow (4MHz), 1 = fast (8MHz)
		  bit 2	  = 0  80287 installed, 1= no NDP installed
		  bit 1-0      reserved

		 AT keyboard controller output port bit definitions
		  bit 7 =    keyboard data output
		  bit 6 =    keyboard clock output
		  bit 5 = 0  input buffer full
		  bit 4 = 0  output buffer empty
		  bit 3 =    reserved (see note)
		  bit 2 =    reserved (see note)
		  bit 1 =    gate A20
		  bit 0 =    system reset
		Note:	bits 2 and 3 are the turbo speed switch or password
			  lock on Award/AMI/Phoenix BIOSes.  These bits make
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          use of nonstandard keyboard controller BIOS
          functionality to manipulate
            pin 23 (8041 port 22) as turbo switch for AWARD
            pin 35 (8041 port 15) as turbo switch/pw lock for
                Phoenix

0060   r/w    KB controller data port or keyboard input buffer (ISA, EISA)
              should only be read from after status port bit0 = 1
              should only be written to if status port bit1 = 0
              keyboard commands (data also goes to port 0060):
               E6     sngl  set mouse scaling to 1:1
               E7     sngl  set mouse scaling to 2:1
               E8     dbl   set mouse resolution
                              (00h = 1/mm,01h = 2/mm,02h = 4/mm,03h = 8/mm)
               E9     sngl  get mouse information
                              read two status bytes:
                                byte 0
                                      bit 7 unused
                                      bit 6 remote rather than stream mode
                                      bit 5 mouse enabled
                                      bit 4 scaling set to 2:1
                                      bit 3 unused
                                      bit 2 left button pressed
                                      bit 1 unused
                                      bit 0 right button pressed
                                byte 1: resolution
               ED     dbl   set/reset mode indicators Caps Num Scrl
                              bit 2 = CapsLk, bit 1 = NumLk, bit 0 = ScrlLk
               EE     sngl  diagnostic echo. returns EE.
               EF     sngl  NOP (No OPeration). reserved for future use
               F0     dbl   get/set scan code set
                              00h get current set
                              01h scancode set 1 (except Type 2 ctrlr)
                              02h scancode set 2 (default)
                              03h scancode set 3
               F2     sngl  read keyboard ID (read two ID bytes)
               F2     sngl  read mouse ID (read two ID bytes)
               F3     dbl   set typematic rate/delay
               F3     dbl   set mouse sample rate in reports per second
               F4     sngl  enable keyboard
               F4     sngl  enable mouse
               F5     sngl  disable keyboard. set default parameters
               F5     sngl  disable mouse, set default parameters
               F6     sngl  set default parameters
               F7     sngl  [MCA] set all keys to typematic (scancode set 3)
               F8     sngl  [MCA] set all keys to make/release
               F9     sngl  [MCA] set all keys to make only
               FA     sngl  [MCA] set all keys to typematic/make/release
               FB     sngl  [MCA] set al keys to typematic
               FC     dbl   [MCA] set specific key to make/release
               FD     dbl   [MCA] set specific key to make only
               FE     sngl  resend last scancode
               FF     sngl  perform internal power-on reset function
               FF     sngl  reset mouse
              Note:   must issue command D4h to port 64h first to access
                        mouse functions


0060   r      KeyBoard or KB controller data output buffer (via PPI on XT)

0061   w      KB controller port B (ISA, EISA)   (PS/2 port A is at 0092)
              system control port for compatibility with 8255
               bit 7  (1= IRQ 0 reset )
               bit 6-4    reserved
               bit 3 = 1  channel check enable
               bit 2 = 1  parity check enable
               bit 1 = 1  speaker data enable
               bit 0 = 1  timer 2 gate to speaker enable

0061   r      KB controller port B control register (ISA, EISA)
              system control port for compatibility with 8255
               bit 7   parity check occurred
               bit 6   channel check occurred
               bit 5   mirrors timer 2 output condition
               bit 4   toggles with each refresh request
               bit 3   channel check status
               bit 2   parity check status
               bit 1   speaker data status
               bit 0   timer 2 gate to speaker status

0061   w      PPI  Programmable Peripheral Interface 8255 (XT only)
              system control port
               bit 7 = 1  clear keyboard
               bit 6 = 0  hold keyboard clock low
               bit 5 = 0  I/O check enable
               bit 4 = 0  RAM parity check enable
               bit 3 = 0  read low switches
               bit 2      reserved, often used as turbo switch
               bit 1 = 1  speaker data enable
               bit 0 = 1  timer 2 gate to speaker enable

0062   r/w    PPI (XT only)
               bit 7 = 1  RAM parity check
               bit 6 = 1  I/O channel check
               bit 5 = 1  timer 2 channel out
               bit 4      reserved
               bit 3 = 1  system board RAM size type 1
               bit 2 = 1  system board RAM size type 2
               bit 1 = 1  coprocessor installed
               bit 0 = 1  loop in POST

0063   r/w    PPI (XT only) command mode register  (read dipswitches)
               bit 7-6 = 00  1 diskette drive
                       = 01  2 diskette drives
                       = 10  3 diskette drives
                       = 11  4 diskette drives
               bit 5-4 = 00  reserved
                       = 01  40*25 color (mono mode)
                       = 10  80*25 color (mono mode)
                       = 11  MDA 80*25
               bit 3-2 = 00  256K (using 256K chips)
                       = 01  512K (using 256K chips)
                       = 10  576K (using 256K chips)
                       = 11  640K (using 256K chips)
               bit 3-2 = 00  64K  (using 64K chips)
                       = 01  128K (using 64K chips)
                       = 10  192K (using 64K chips)
                       = 11  256K (using 64K chips)
               bit 1-0       reserved

0064   r      KB controller read status (ISA, EISA)
               bit 7 = 1 parity error on transmission from keyboard
               bit 6 = 1 receive timeout
               bit 5 = 1 transmit timeout
               bit 4 = 0 keyboard inhibit
               bit 3 = 1 data in input register is command
                       0 data in input register is data
               bit 2   system flag status: 0=power up or reset  1=selftest OK
               bit 1 = 1 input buffer full (input 60/64 has data for 8042)
               bit 0 = 1 output buffer full (output 60 has data for system)

0064   r      KB controller read status (MCA)
               bit 7 = 1 parity error on transmission from keyboard
               bit 6 = 1 general timeout
               bit 5 = 1 mouse output buffer full
               bit 4 = 0 keyboard inhibit
               bit 3 = 1 data in input register is command
                       0 data in input register is data
               bit 2   system flag status: 0=power up or reset  1=selftest OK
               bit 1 = 1 input buffer full (input 60/64 has data for 804x)
               bit 0 = 1 output buffer full (output 60 has data for system)

0064   r      KB controller read status by Compaq
               bit 7 = 1 parity error detected (11-bit format only). If an
                         error is detected, a Resend command is sent to the
                         keyboard once only, as an attempt to recover.
               bit 6 = 1 receive timeout. transmission didn't finish in 2mS.
               bit 5 = 1 transmission timeout error
                           bit 5,6,7  cause
                               1 0 0  No clock
                               1 1 0  Clock OK, no response
                               1 0 1  Clock OK, parity error
               bit 4 = 0 security lock engaged
               bit 3 = 1 data in OUTPUT register is command
                       0 data in OUTPUT register is data
               bit 2   system flag status: 0=power up or reset  1=soft reset
               bit 1 = 1 input buffer full (output 60/64 has data)
               bit 0 = 0 no new data in buffer (input 60 has data)

0064   w      KB controller input buffer (ISA, EISA)
              KB controller commands (data goes to port 0060):
               20     read  read byte zero of internal RAM, this is the
                            last KB command send to 804x
                    Compaq  Put current command byte on port 0060
                              command structure:
                              bit 7   reserved
                              bit 6 = 1 convert KB codes to 8086 scan codes
                              bit 5 = 0 use 11-bit codes, 1=use 8086 codes
                              bit 4 = 0 enable keyboard, 1=disable keyboard
                              bit 3 = 1 ignore security lock state
                              bit 2     this bit goes into bit2 status reg.
                              bit 1 = 0 reserved
                              bit 0 = 1 generate int. when output buffer full
               21-3F  read  reads the byte specified in the lower 5 bits of
                            the command in the 804x's internal RAM
               60-7F  dbl   writes the data byte to the address specified in
                            the 5 lower bits of the command.

                            Alternate description KB IO command 60 summary:
                             bit7 = 0 reserved
                             bit6 =   IBM PC compatibility mode
                             bit5 =   IBM PC mode
                             bit4 =   disable kb
                             bit3 =   inhibit override
                             bit2 =   system flag
                             bit1 = 0 reserved
                             bit0 =   enableoutput buffer full interrupt

               60   Compaq  Load new command (60 to [64], command to [60])
               A1   Compaq  unknown speedfunction ??
               A2   Compaq  unknown speedfunction ??
               A3   Compaq  Enable system speed control
               A4     MCA   check if password installed
               A4   Compaq  Toggle speed
               A5     MCA   load password
               A5   Compaq  Special reed. the 8042 places the real values
                            of port 2 except for bits 4 and 5 wich are given
                            a new definition in the output buffer. No output
                            buffer full is generated.
                              if bit 5 = 0, a 9-bit keyboard is in use
                              if bit 5 = 1, an 11-bit keyboard is in use
                              if bit 4 = 0, outp-buff-full interrupt disabled
                              if bit 4 = 1, output-buffer-full int. enabled
               A6     MCA   check password
               A6   Compaq  unknown speedfunction ??
               A7     MCA   disable mouse port
               A8     MCA   enable mouse port
               A9     MCA   test mouse port
               AA     sngl  initiate self-test. will return 55 to data port
                    Compaq  Initializes ports 1 and 2, disables the keyboard
                            and clears the buffer pointers. It then places
                            55 in the output buffer.
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                AB     sngl  initiate interface test. result values:
                              0 = no error
                              1 = keyboard clock line stuck low
                              2 = keyboard clock line stuck high
                              3 = keyboard data line is stuck low
                              4 = keyboard data line stuck high
                     Compaq   5 = Compaq diagnostic feature
                AC     read  diagnostic dump. the contents of the 804x RAM,
                             output port, input port, status word are send.
                AD     sngl  disable keyboard (sets bit 4 of commmand byte)
                AE     sngl  enable keyboard  (resets bit 4 of commmand byte)
                AF     AWARD Enhanced Command: read keyboard version
                C0     read  read input port
                     Compaq  Places status of input port in output buffer. use
                             this command only when the output buffer is empty
                C1     MCA   Enhanced Command: poll input port Low nibble
                C2     MCA   Enhanced Command: poll input port High nibble
                D0     read  read output port
                     Compaq  Places byte in output port in output buffer. use
                             this command only when the output buffer is empty
                D1     dbl   write output port. next byte written  to 0060
                             will be written to the 804x output port; the
                             original IBM AT and many compatibles use bit 1 of
                             the output port to control the A20 gate.
                     Compaq  The system speed bits are not set by this command
                             use commands A1-A6 (!) for speed functions.
                D2     MCA   Enhanced Command: write keyboard output buffer
                D3     MCA   Enhanced Command: write pointing device out.buf.
                D4     MCA   write to mouse
                D4     AWARD Enhanced Command: write to auxiliary device
                DD     sngl  disable address line A20 (HP Vectra only???)
                             default in Real Mode
                DF     sngl  enable address line A20 (HP Vectra only???)
                E0     read  read test inputs.
                               bit0 = kbd clock, bit1 = kbd data
                Exxx   AWARD Enhanced Command: active output port
                ED   Compaq  This is a two part command to control the state
                             of the NumLock CpasLock and ScrollLock LEDs
                             The second byte contains the state to set LEDs.
                               bit 7-3    reserved. should be set to 0.
                               bit 2 = 0  Caps Lock LED off
                               bit 1 = 0  Num Lock LED off
                               bit 0 = 0  Scroll Lock LED off
                F0-FF  sngl  pulse output port low for 6 microseconds.
                             bits 0-3 contain the mask for the bits to be
                             pulsed. a bit is pulsed if its mask bit is zero.
                             bit0=system reset. Don't set to zero. Pulse only!

general note:    Keyboard controllers are widely different from each other.
                 You cannot generally exchange them between different machines.
note on Award:   Derived from Award's Enhanced KB controller advertising sheet.
note on Compaq:  Derived from the Compaq Deskpro 386 Tech. Ref. Guide.

0065     r       communications port (Olivetti M24)

0068     w       HP-Vectra  control buffer (HP commands)
0069     r       HP-Vectra  SVC (keyboard request SerViCe port)
006A     w       HP-Vectra  clear processing, done

006C-006F        HP-HIL  (Human Interface Link = async. serial inputs 0-7)

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0070-007F ----  CMOS RAM/RTC (Real Time Clock  MC146818)

0070     w       CMOS RAM index register port (ISA, EISA)
                  bit 7   = 1  NMI disabled
                          = 0  NMI enabled
                  bit 6-0      CMOS RAM index (64 bytes, sometimes 128 bytes)

                 any write to 0070 should be followed by an action to 0071
                 or the RTC wil be left in an unknown state.

0071     r/w     CMOS RAM data port (ISA, EISA)
                 RTC registers:
                 00     current second in BCD
                 01     alarm second   in BCD
                 02     current minute in BCD
                 03     alarm minute   in BCD
                 04     current hour in BCD
                 05     alarm hour   in BCD
                 06     day of week  in BCD
                 07     day of month in BCD
                 08     month in BCD
                 09     year  in BCD (00-99)
                 0A     status register A
                         bit 7 = 1  update in progress
                         bit 6-4 divider that identifies the time-based
                                  frequency
                         bit 3-0 rate selection output  frequency and int. rate
                 0B     status register B
                         bit 7 = 0  run
                               = 1  halt
                         bit 6 = 1  enable periodic interrupt
                         bit 5 = 1  enable alarm interrupt
                         bit 4 = 1  enable update-ended interrupt
                         bit 3 = 1  enable square wave interrupt
                         bit 2 = 1  calendar is in binary format
                               = 0  calendar is in BCD format
                         bit 1 = 1  24-hour mode
                               = 0  12-hour mode
                         bit 0 = 1  enable daylight savings time. only in USA.
                                    useless in Europe. Some DOS versions clear
                                    this bit when you use the DAT/TIME command.
                 0C     status register C
                         bit 7 =    interrupt request flag
                         bit 6 =    peridoc interrupt flag
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         bit 5 =    alarm interrupt flag
         bit 4 =    update interrupt flag
         bit 3-0    reserved
0D     status register D
         bit 7 = 1  Real-Time Clock has power
         bit 6-0    reserved
0E     diagnostics status byte
         bit 7 = 0  RTC lost power
         bit 6 = 1  CMOS RAM checksum bad
         bit 5 = 1  invalid configuration information at POST
         bit 4 = 1  memory size error at POST
         bit 3 = 1  fixed disk/adapter failed initialization
         bit 2 = 1  CMOS RAM time found invalid
         bit 1 = 1  adapters do not match configuration (EISA)
         bit 0 = 1  time out reading an adapter ID (EISA)
0F     shutdown status byte
         00 = normal execution of POST
         01 = chip set initialization for real mode reentry
         04 = jump to bootstrap code
         05 = issue an EOI an JMP to Dword ptr at 40:67
         06 = JMP to Dword ptrv at 40:67 without EOI
         07 = return to INT15/87 (block move)
         08 = return to POST memory test
         09 = return to INT15/87 (block move)
         0A = JMP to Dword ptr at 40:67 without EOI
         0B = return IRETS through 40:67
10     diskette drive type for A: and B:
         bit 7-4  drive type of drive 0
         bit 3-0  drive type of drive 1
                = 0000      no drive
                = 0001      360K
                = 0010      1M2
                = 0011      720K
                = 0100      1M44
                = 0101-1111 reserved
11     reserved / AMI Extended CMOS setup (AMI Hi-Flex BIOS)
         bit 7   = 1     Typematic Rate Programming
         bit 6-5 = 00    Typematic Rate Delay 250 mSec
         bit 4-0 = 00011 Typematic Rate 21.8 Chars/Sec
12     fixed disk drive type for drive 0 and drive 1
         bit 7-4  drive type of drive 0
         bit 3-0  drive type of drive 1
                 if either of the nibbles equals 0F, then bytes
                 19 an 1A are valid
13     reserved / AMI Extended CMOS setup (AMI Hi-Flex BIOS)
         bit 7 = 1  Mouse Support Option
         bit 6 = 1  Above 1 MB Memory Test disable
         bit 5 = 1  Memory Test Tick Sound disable
         bit 4 = 1  Memory Parity Error Check enable
         bit 3 = 1  Hit <ESC> Message Display disabled
         bit 2 = 1  Hard Disk Type 47 Data Area at address 0:300
         bit 1 = 1  Wait For <F1> If Any Error enabled
         bit 0 = 1  System Boot Up Num Lock is On
14     equipment byte
         bit 7-6   diskette drives installed
                = 00  1 drive installed
                = 01  2 drives installed
                = 10  reserved
                = 11  reserved
         bit 5-4   primary display
                = 00  adapter card with option ROM
                = 01  40*25 color
                = 10  80*25 color
                = 11  monochrome
         bit 3-2   reserved
         bit 1   = 1  coprocessor installed (non-Weitek)
         bit 0        diskette drive avaliable for boot
15     LSB of systemn base memory in Kb
16     MSB of systemn base memory in Kb
17     LSB of total extended memory in Kb
18     MSB of total extended memory in Kb
19     drive C extension byte
1A     drive D extension byte
1B-27 reserved
1B/1C word to 82335 RC1 roll compare register at [24]
         (Phoenix)
1D/1E word to 82335 RC2 roll compare register at [26]
         (Phoenix)
28     HP-Vectra checksum over 29-2D
29-2D reserved
29/2A word to Intel 82335 CC0 compare register at
        [28](Phoenix)
2B/2C word send to 82335 CC1 compare register at [2A]
         (Phoenix)
2D     AMI Extended CMOS setup (AMI Hi-Flex BIOS)
       (Phoenix BIOS checks for the values AA or CC)
         bit 7 = 1  Weitek Processor Absent
         bit 6 = 1  Floppy Drive Seek At Boot disabled
         bit 5 = 1  System Boot Up Sequence  C:, A:
         bit 4 = 1  System Boot Up Speed is high
         bit 3 = 1  Cache Memory enabled
         bit 2 = 1  Internal Cache Memory  <1>
         bit 1-0    reserved
2E     CMOS MSB checksum over 10-2D
2F     CMOS LSB checksum over 10-2D
30     LSB of extended memory found above 1Mb at POST
31     MSB of extended memory found above 1Mb at POST
32     date century in BCD
33     information flags
         bit4 = bit4 from CPU register CR0   (Phoenix)
                this bit is only known as INTEL RESERVED
34-3F reserved
34     bit4 bit5 (Phoenix BIOS)
3D/3E word to 82335 MCR memory config register at
        [22](Phoenix)
3D     bit3      base memsize 512/640  (Phoenix)
```

```
                3E     bit7 = 1  relocate enable       (Phoenix)
                       bit1 = 1  shadow video enable   (Phoenix)
                       bit0 = 1  shadow BIOS enable    (Phoenix)

                User Definable Drive Parameters are also stored in CMOS RAM:

                AMI (386sx BIOS 1989) first user definable drive (type 47)
                 1B  L cylinders
                 1C  H cylinders
                 1D  heads
                 1E  L Write Precompensation Cylinder
                 1F  H Write Precompensation Cylinder
                 20  ??
                 21  L cylinders parking zone
                 22  H cylinders parking zone
                 23  sectors

                AMI (386sx BIOS 1989) second user definable drive (type 48)
                 24  L cylinders
                 25  H cylinders
                 26  heads
                 27  L Write Precompensation Cylinder
                 28  H Write Precompensation Cylinder
                 29  ??
                 2A  L cylinders parking zone
                 2B  H cylinders parking zone
                 2C  sectors

                Phoenix (386BIOS v1.10.03 1988) 1st user definable drv (type48)
                 20  L cylinders
                 21  H cylinders
                 22  heads
                 23  L Write Precompensation Cylinder
                 24  H Write Precompensation Cylinder
                 25  L cylinders parking zone
                 26  H cylinders parking zone
                 27  sectors

                Phoenix (386BIOS v1.10.03 1988) 2nd user definable drv (type49)
                (when PS/2-style password option is not used)
                 35  L cylinders
                 36  H cylinders
                 37  heads
                 38  L Write Precompensation Cylinder
                 39  H Write Precompensation Cylinder
                 3A  L cylinders parking zone
                 3B  H cylinders parking zone
                 3C  sectors

--------------------------------------------------------------------------------
0080    w       Manufacturing Diagnostics port

--------------------------------------------------------------------------------
0080-008F ----  DMA page registers   (74612)

0080    r/w     extra page register (temporary storage)
0081    r/w     DMA channel 2 address byte 2
0082    r/w     DMA channel 3 address byte 2
0083    r/w     DMA channel 1 address byte 2
0084    r/w     extra page register
0085    r/w     extra page register
0086    r/w     extra page register
0087    r/w     DMA channel 0 address byte 2
0088    r/w     extra page register
0089    r/w     DMA channel 6 address byte 2
0089    r/w     DMA channel 7 address byte 2
0089    r/w     DMA channel 5 address byte 2
008C    r/w     extra page register
008D    r/w     extra page register
008E    r/w     extra page register
008F    r/w     DMA refresh page register

--------------------------------------------------------------------------------
00A0-00AF ----  PIC 2   (Programmable Interrupt Controller 8259)

00A0    r/w     NMI mask register (XT)

00A0    r/w     PIC 2  same as 0020 for PIC 1
00A1    r/w     PIC 2  same as 0021 for PIC 1 except for OCW1:
                 bit 7 = 0  reserved
                 bit 6 = 0  enable fixed disk interrupt
                 bit 5 = 0  enable coprocessor exception interrupt
                 bit 4 = 0  enable mouse interrupt
                 bit 3 = 0  reserved
                 bit 2 = 0  reserved
                 bit 1 = 0  enable redirect cascade
                 bit 0 = 0  enable real-time clock interrupt

--------------------------------------------------------------------------------
00C0-00DF ----  DMA 2   (second Direct Memory Access controller 8237)

00C0    r/w     DMA channel 4 memory address bytes 1 and 0 (low) (ISA, EISA)
00C2    r/w     DMA channel 4 transfer count bytes 1 and 0 (low) (ISA, EISA)
00C4    r/w     DMA channel 5 memory address bytes 1 and 0 (low) (ISA, EISA)
00C6    r/w     DMA channel 5 transfer count bytes 1 and 0 (low) (ISA, EISA)
00C8    r/w     DMA channel 6 memory address bytes 1 and 0 (low) (ISA, EISA)
00CA    r/w     DMA channel 6 transfer count bytes 1 and 0 (low) (ISA, EISA)
00CC    r/w     DMA channel 7 memory address byte 0 (low), then 1 (ISA, EISA)
00CE    r/w     DMA channel 7 transfer count byte 0 (low), then 1 (ISA, EISA)

00D0    r       DMA channel 4-7 status register (ISA, EISA)
                 bit 7 = 1  channel 7 request
                 bit 6 = 1  channel 6 request
                 bit 5 = 1  channel 5 request
                 bit 4 = 1  channel 4 request
                 bit 3 = 1  terminal count on channel 7
                 bit 2 = 1  terminal count on channel 6
                 bit 1 = 1  terminal count on channel 5
                 bit 0 = 1  terminal count on channel 4

00D0    w       DMA channel 4-7 command register (ISA, EISA)
                 bit 7 = 1  DACK sense active high
                       = 0  DACK sense active low
                 bit 6 = 1  DREQ sense active high
                       = 0  DREQ sense active low
                 bit 5 = 1  extended write selection
                       = 0  late write selection
                 bit 4 = 1  rotating priority
                       = 0  fixed priority
                 bit 3 = 1  compressed timing
                       = 0  normal timing
                 bit 2 = 0  enable controller
                 bit 1 = 1  enable memory-to-memory transfer
                 bit 0      .....

00D2    w       DMA channel 4-7 write request register (ISA, EISA)

00D4    w       DMA channel 4-7 write single mask register (ISA, EISA)
                 bit 7-3    reserved
                 bit 2   = 0  clear mask bit
                         = 1  set mask bit
                 bit 1-0 = 00 channel 4 select
                         = 01 channel 5 select
                         = 10 channel 6 select
                         = 11 channel 7 select

00D6    w       DMA channel 4-7 mode register (ISA, EISA)
                 bit 7-6 = 00  demand mode
                         = 01  single mode
                         = 10  block mode
                         = 11  cascade mode
                 bit 5   = 0   address increment select
                         = 1   address decrement select
                 bit 4   = 0   autoinitialisation disable
                         = 1   autoinitialisation enable
                 bit 3-2 = 00  verify operation
                         = 01  write to memory
                         = 10  read from memory
                         = 11  reserved
                 bit 1-0 = 00  channel 4 select
                         = 01  channel 5 select
                         = 10  channel 6 select
                         = 11  channel 7 select

00D8    w       DMA channel 4-7 clear byte pointer flip-flop (ISA, EISA)
00DA    r       DMA channel 4-7 read temporary register (ISA, EISA)
00DA    w       DMA channel 4-7 master clear (ISA, EISA)
00DC    w       DMA channel 4-7 clear mask register (ISA, EISA)
00DE    w       DMA channel 4-7 write mask register (ISA, EISA)

--------------------------------------------------------------------------------
00F0-00FF ----  coprocessor (8087..80387)

00F0    w       math coprocessor clear busy latch
00F1    w       math coprocessor reset
00F8    r/w     opcode transfer
00FA    r/w     opcode transfer
00FC    r/w     opcode transfer

--------------------------------------------------------------------------------
0130-0133 ----  Adaptec 154xB/154xC SCSI adapter.
                alternate address at 0134, 0230, 0234, 0330 and 0334

--------------------------------------------------------------------------------
0134-0137 ----  Adaptec 154xB/154xC SCSI adapter.
                alternate address at 0130, 0230, 0234, 0330 and 0334

--------------------------------------------------------------------------------
0140-014F ----  SCSI (alternate Small Computer System Interface) adapter
                (1st at 0340-034F)

--------------------------------------------------------------------------------
0178-0179 ----  Power Management

0178    w       index selection for data port
0179    r/w     power management data

--------------------------------------------------------------------------------
0200-020F ----  Game port reserved I/O address space
0200-0207 ----  Game port, eight identical addresses on some boards

0201    r       read joystick position and status
                 bit 7  status B joystick button 2 / D paddle button
                 bit 6  status B joystick button 1 / C paddle button
                 bit 5  status A joystick button 2 / B paddle button
                 bit 4  status A joystick button 1 / A paddle button
                 bit 3  B joystick Y coordinate    / D paddle coordinate
                 bit 2  B joystick X coordinate    / C paddle coordinate
                 bit 1  A joystick Y coordinate    / B paddle coordinate
                 bit 0  A joystick X coordinate    / A paddle coordinate

        w       fire joysticks four one-shots

-------------------------------------------------------------------------------
0220-0223 ---- Sound Blaster / Adlib port

0220    r/w     Left speaker -- Status / Address port
0221    w       Left speaker -- Data port
0222    r/w     Right speaker -- Status / Address port
                Address:
                    01 -- Enable waveform control
```

```
                    02 -- Timer #1 data
                    03 -- Timer #2 data
                    04 -- Timer control flags
                    08 -- Speech synthesis mode
                 20-35 -- Amplitude Modulation / Vibrato
                 40-55 -- Level key scaling / Total level
                 60-75 -- Attack / Decay rate
                 80-95 -- Sustain / Release rate
                 A0-B8 -- Octave / Frequency Number
                 C0-C8 -- Feedback / Algorithm
                 E0-F5 -- Waveform Selection
0223    w       Right speaker -- Data port

SeeAlso: 0388-0389

--------------------------------------------------------------------------------
0220-0227 ----  Soundblaster PRO and SSB 16 ASP

--------------------------------------------------------------------------------
0220-022F ----  Soundblaster PRO 2.0

--------------------------------------------------------------------------------
0220-022F ----  Soundblaster PRO 4.0
0220    r       left FM status port
0220    w       left FM music register address port (index)
0221    r/w     left FM music data port
0222    r       right FM status port
0222    w       right FM music register address port (index)
0223    r/w     right FM music data port
0224    w       mixer register address port (index)
0225    r/w     mixer data port
0226    w       DSP reset
0228    r       FM music status port
0228    w       FM music register address port (index)
0229    w       FM music data port
022A    r       DSP read data (voice I/O and Midi)
022C    w       DSP write data / write command
022C    r       DSP write buffer status (bit 7)
022E    r       DSP data available status (bit 7)

                The FM music is accessible on 0388/0389 for compatibility.

--------------------------------------------------------------------------------
0230-0233 ----  Adaptec 154xB/154xC SCSI adapter.
                alternate address at 0130, 0134, 0230, 0330 and 0334

--------------------------------------------------------------------------------
0234-0237 ----  Adaptec 154xB/154xC SCSI adapter.
                alternate address at 0130, 0134, 0230, 0330 and 0334

--------------------------------------------------------------------------------
0278-027E ----  parallel printer port, same as 0378 and 03BC

0278    w       data port
0279    r/w     status port
027A    r/w     control port

--------------------------------------------------------------------------------
02B0-02DF ----  alternate EGA,  primary EGA at 03C0

--------------------------------------------------------------------------------
02E8-02EF ----  serial port, same as 02F8, 03E8 and 03F8

--------------------------------------------------------------------------------
02E8-02EF ----  8514/A and compatible video cards (e.g. ATI Graphics Ultra)

02E8    r       display status
02E8    w       horizontal total
02EA    w       DAC mask
02EB    w       DAC read index
02EC    w       DAC write index
02ED    w       DAC data

--------------------------------------------------------------------------------
02F8-02FF ----  serial port, same as 02E8, 03E8 and 03F8

02F8    w       transmitter holding register
02F8    r       receiver buffer register
        r/w     divisor latch, low byte   when DLAB=1
02F9    r/w     divisor latch, high byte  when DLAB=1
        r/w     interrupt enable register when DLAB=0
02FA    r       interrupt identification register
02FB    r/w     line control register
02FC    r/w     modem control register
02FD    r       line status register
02FF    r/w     scratch register

--------------------------------------------------------------------------------
0300-0301 ---- Soundblaster 16 ASP MPU-Midi

--------------------------------------------------------------------------------
0300-031F ----  prototype cards
                Periscope hardware debugger

--------------------------------------------------------------------------------
0330-0331 ----  MIDI interface

--------------------------------------------------------------------------------
0330-0333 ----  Adaptec 154xB/154xC SCSI adapter. default address.
                alternate address at 0130, 0134, 0230, 0234 and 0334

--------------------------------------------------------------------------------
0334-0337 ----  Adaptec 154xB/154xC SCSI adapter.
                alternate address at 0130, 0134, 0230, 0234 and 0330

--------------------------------------------------------------------------------
0338      ----  AdLib soundblaster card

--------------------------------------------------------------------------------
0340-034F ----  SCSI (1st Small Computer System Interface) adapter
                (alternate at 0140-014F)

--------------------------------------------------------------------------------
0370-0377 ----  FDC 2  (2nd Floppy Disk Controller)     first FDC at 03F0
                (8272, 8272A, NEC765)
                (82072, 82077AA for perpendicular recording at 2.8Mb)

0370    r       diskette Extra High Density controller board jumpers (AT)
0370    r       diskette controller status A (PS/2, PS/2 model 30)
0371    r       diskette controller status B (PS/2, PS/2 model 30)
0372    w       diskette controller DOR (Digital Output Register)
0374    r       diskette controller main status register
0374    w       diskette controller datarate select register
0375    r/w     diskette controller command/data register
0376    r/w     (2nd FIXED disk controller data register)
0377    r       diskette controller DIR (Digital Input Register)
0377    w       select register for diskette data transfer rate

--------------------------------------------------------------------------------
0378-037A ----  parallel printer port, same as 0278 and 03BC

0378    w       data port
0379    r/w     status port
037A    r/w     control port

-------------------------------------------------------------------------------
0388-0389 ---- Sound Blaster / Adlib port

0388    r/w     Both Speakers -- Status / Address port
                Address:
                     01 -- Enable waveform control
                     02 -- Timer #1 data
                     03 -- Timer #2 data
                     04 -- Timer control flags
                     08 -- Speech synthesis mode
                  20-35 -- Amplitude Modulation / Vibrato
                  40-55 -- Level key scaling / Total level
                  60-75 -- Attack / Decay rate
                  80-95 -- Sustain / Release rate
                  A0-B8 -- Octave / Frequency Number
                  C0-C8 -- Feedback / Algorithm
                  E0-F5 -- Waveform Selection
0389    w       Data port

SeeAlso: 0220-0223

--------------------------------------------------------------------------------
0388-0389 ---- Soundblaster PRO FM-Chip
0388-038B ---- Soundblaster 16 ASP FM-Chip

--------------------------------------------------------------------------------
03B0-03BF ----  MDA  (Monochrome Display Adapter based on 6845)

03B0            same as 03B4
03B1            same as 03B5
03B2            same as 03B4
03B3            same as 03B5
03B4    w       MDA CRT index register   (EGA/VGA)
                selects which register (0-11h) is to be accessed through 3B5
03B5    r/w     MDA CRT data register    (EGA/VGA)
                selected by port 3B4. registers C-F may be read
                 00  horizontal total
                 01  horizontal displayed
                 02  horizontal sync position
                 03  horizontal sync pulse width
                 04  vertical total
                 05  vertical displayed
                 06  vertical sync position
                 07  vertical sunc pulse width
                 08  interlace mode
                 09  maximum scan lines
                 0A  cursor start
                 0B  cursor end
                 0C  start address high
                 0D  start address low
                 0E  cursor location high
                 0F  cursor location low
                 10  light pen high
                 11  light pen low
03B6            same as 03B4
03B7            same as 03B5
03B8    r/w     MDA mode control register
                 bit 7 not used
                 bit 6 not used
                 bit 5 enable blink
                 bit 4 not used
                 bit 3 video enable
                 bit 2 not used
                 bit 1 not used
                 bit 0 high resolution mode

03B9            reserved for color select register on color adapter

03BA    r       CRT status register      EGA/VGA: input status 1 register
                 bit 7   (MSD says) if this bit changes within 8000h reads then
                  bit 6-4 = 000 = adapter is Hercules or compatible
                            001 = adapter is Hercules+
                            101 = adapter is Hercules InColor
                                  else: adapter is unknown
                 bit 3   black/white video
                 bit 2-1 reserved
                 bit 0   horizontal drive
```

```
03BA    w       EGA/VGA feature control register

03BB            reserved for light pen strobe reset

--------------------------------------------------------------------------------
03BC-03BF ----  parallel printer port, same as 0278 and 0378

03BC    w       data port
03BD    r/w     status port
                 bit 7 = 0  busy
                 bit 6 = 0  acknowledge
                 bit 5 = 1  out of paper
                 bit 4 = 1  printer is selected
                 bit 3 = 0  error
                 bit 2 = 0  IRQ has occurred
                 bit 1-0    reserved

03BE    r/w     control port
                 bit 7-5    reserved
                 bit 4 = 1  enable IRQ
                 bit 3 = 1  select printer
                 bit 2 = 0  initialize printer
                 bit 1 = 1  automatic line feed
                 bit 0 = 1  strobe

--------------------------------------------------------------------------------
03BF    r/w     Hercules configuration switch register
                 bit 7-2
                 bit 1 = 0  disables upper 32K of graphics mode buffer
                         1  enables upper 32K of graphics mode buffer
                 bit 0 = 0  prevents graphics mode
                         1  allows graphics mode

--------------------------------------------------------------------------------
03C0-03CF ----  EGA  (1st Enhanced Graphics Adapter)    alternate at 02C0

03C0    (r)/w   EGA VGA ATC index/data register
03C1    r       VGA     other attribute register
03C2    r       EGA VGA input status 0 register
        w       VGA     miscellaneous output register
03C3    r/w     VGA     video subsystem enable (see also port 46E8h)
                        for IBM, motherboard VGA only
03C4    w       EGA     TS index register
        r/w     VGA     sequencer index register
03C5    w       EGA     TS data register
        r/w     VGA     other sequencer register
03C6    r/w     VGA     PEL mask register
03C7    r/w     VGA     PEL address read mode
        r       VGA     DAC state register
03C8    r/w     VGA     PEL address write mode
03C9    r/w     VGA     PEL data register
03CA    w       EGA     graphics 2 position register
        r       VGA     feature control register
03CC    w       EGA     graphics 1 position register
        r       VGA     miscellaneous output register
03CE    w       EGA     GDC index register
        r/w     VGA     graphics address register
03CF    w       EGA     GDC data register
        r/w     VGA     other graphics register

--------------------------------------------------------------------------------
03D0-03DF ----  CGA   (Color Graphics Adapter)

03D0            same as 03D4
03D1            same as 03D5
03D2            same as 03D4
03D3            same as 03D5
03D4    w       CRT (6845) index register   (EGA/VGA)
                selects which register (0-11h) is to be accessed through 3B5
03D5    w       CRT (6845) data register    (EGA/VGA)
                selected by port 3B4. registers C-F may be read
                 (for registers see at 3B5)
03D6            same as 03D4
03D7            same as 03D5
03D8    r/w     CGA mode control register  (except PCjr)
                 bit 7-6      not used
                 bit 5   = 1  blink enabled
                 bit 4   = 1  640*200 graphics mode
                 bit 3   = 1  video enabled
                 bit 2   = 1  monochrome signal
                 bit 1   = 0  text mode
                         = 1  320*200 graphics mode
                 bit 0   = 0  40*25 text mode
                         = 1  80*25 text mode

03D9    r/w     CGA palette register
                 bit 7-6      not used
                 bit 5   = 0 active color set: red, green brown
                         = 1 active color set: cyan, magenta, white
                 bit 4       intense colors in graphics, background colors text
                 bit 3       intense border in 40*25, intense background in
                             320*200, intense foreground in 640*200
                 bit 2       red border in 40*25, red background in 320*200,
                             red foreground in 640*200
                 bit 1       green border in 40*25, green background in
                             320*200, green foreground in 640*200
                 bit 0       blue border in 40*25, blue background in 320*200,
                             blue foreground in 640*200

03DA    r       CGA status register     EGA/VGA: input status 1 register
                 bit 7-4    not used
                 bit 3 = 1   in vertical retrace
                 bit 2 = 1   light pen switch is off
                 bit 1 = 1   positive edge from light pen has set trigger
                 bit 0 = 0   do not use memory
```

```
                       = 1   memory access without interfering with display

03DA    w       EGA/VGA feature control register

03DB    w       clear light pen latch
03DC    r/w     preset light pen latch

03DF            CRT/CPU page register  (PCjr only)

--------------------------------------------------------------------------------
03E8-03EF ----  serial port, same as 02E8, 02F8 and 03F8

--------------------------------------------------------------------------------
03F0-03F7 ----  FDC 1  (1st Floppy Disk Controller)     second FDC at 0370
                (8272, 8272A, NEC765)
                (82072, 82077AA for perpendicular recording at 2.8Mb)

03F0    r       diskette EHD controller board jumper settings (82072AA)
                 bit 7-6      drive 3
                 bit 5-4      drive 2
                 bit 3-2      drive 1
                 bit 1-0      drive 0
                        = 00  1.2Mb
                        = 01  720Kb
                        = 10  2.8Mb
                        = 11  1.4Mb

03F0    r       diskette controller status A (PS/2)
                 bit 7   interrupt pending
                 bit 6   -DRV2  second drive installed
                 bit 5   step
                 bit 4   -track 0
                 bit 3   head 1 select
                 bit 2   -index
                 bit 1   -write protect
                 bit 0   +direction

03F0    r       diskette controller status A (PS/2 model 30)
                 bit 7   interrupt pending
                 bit 6   DRQ
                 bit 5   step F/F
                 bit 4   -track 0
                 bit 3   head 1 select
                 bit 2   +index
                 bit 1   +write protect
                 bit 0   -direction

03F1    r       diskette controller status B (PS/2)
                 bit 7-6  =1 reserved
                 bit 5    drive select (0=A:, 1=B:)
                 bit 4    write data
                 bit 3    read data
                 bit 2    write enable
                 bit 1    motor enable 1
                 bit 0    motor enable 0

03F1    r       diskette controller status B (PS/2 model 30)
                 bit 7    -DRV2 second drive installed
                 bit 6    -DS1
                 bit 5    -DS0
                 bit 4    write data F/F
                 bit 3    read data F/F
                 bit 2    write enable F/F
                 bit 1    -DS3
                 bit 0    -DS2

03F2    w       diskette controller DOR (Digital Output Register)
                 bit 7-6    reserved on PS/2
                 bit 7 = 1  drive 3 motor enable
                 bit 6 = 1  drive 2 motor enable
                 bit 5 = 1  drive 1 motor enable
                 bit 4 = 1  drive 0 motor enable
                 bit 3 = 1  diskette DMA enable (reserved PS/2)
                 bit 2 = 1  FDC enable  (controller reset)
                       = 0  hold FDC at reset
                 bit 1-0    drive select (0=A 1=B ..)

03F3            tape drive register (on the 82077AA)
                 bit 7-2      reserved, tri-state
                 bit 1-0      tape select
                        = 00  none, drive 0 cannot be a tape drive.
                        = 01  drive1
                        = 10  drive2
                        = 11  drive3

03F4    r       diskette controller main status register
                 bit 7 = 1  RQM  data register is ready
                        0  no access is permitted
                 bit 6 = 1  transfer is from controller to system
                        0  transfer is from system to controller
                 bit 5 = 1  non-DMA mode
                 bit 4 = 1  diskette controller is busy
                 bit 3 = 1  drive 3 busy (reserved on PS/2)
                 bit 2 = 1  drive 2 busy (reserved on PS/2)
                 bit 1 = 1  drive 1 busy (= drive is in seek mode)
                 bit 0 = 1  drive 0 busy (= drive is in seek mode)
                Note:   in non-DMA mode, all data transfers occur through
                         port 03F5h and the status registers (bit 5 here
                         indicates data read/write rather than than
                         command/status read/write)

03F4    w       diskette controller data rate select register
                 bit 7   = 1  S/W reset
                 bit 6   = 1  power down
                 bit 5   = 0  reserved
                 bit 4-2      write precompensation, 000 default
```

```
            bit 1-0      data rate select
                    = 00  500 Kb/s (MFM)
                    = 01  300 Kb/s (MFM)
                    = 10  250 Kb/s (MFM)
                    = 11  1   Mb/s (MFM)

03F5    r       diskette command/data register 0 (ST0)
                 bit 7-6      last command status
                        = 00  command terminated successfully
                        = 01  command terminated abnormally
                        = 10  invalid command
                        = 11  terminated abnormally by change in ready signal
                 bit 5   = 1  seek completed
                 bit 4   = 1  equipment check occurred after error
                 bit 3   = 1  not ready
                 bit 2   = 1  head number at interrupt
                 bit 1-0 = 1  unit select (0=A 1=B .. )
                              (on PS/2  01=A  10=B)

                status register 1 (ST1)
                 bit 7      end of cylinder; sector# greater then sectors/track
                 bit 6 = 0
                 bit 5 = 1  CRC error in ID or data field
                 bit 4 = 1  overrun
                 bit 3 = 0
                 bit 2 = 1  sector ID not found
                 bit 1 = 1  write protect detected during write
                 bit 0 = 1  ID address mark not found

                status register 2 (ST2)
                 bit 7 = 0
                 bit 6 = 1  deleted Data Address Mark detected
                 bit 5 = 1  CRC error in data
                 bit 4 = 1  wrong cylinder detected
                 bit 3 = 1  scan command equal condition satisfied
                 bit 2 = 1  scan command failed, sector not found
                 bit 1 = 1  bad cylinder, ID not found
                 bit 0 = 1  missing Data Address Mark

                status register 3 (ST3)
                 bit 7      fault status signal
                 bit 6      write protect status
                 bit 5      ready status
                 bit 4      track zero status
                 bit 3      two sided status signal
                 bit 2      side select (head select)
                 bit 1-0    unit select (0=A 1=B .. )

03F5    w       diskette command register.  The commands summarized here are
                mostly multibyte commands. This is for brief recognition only.

                        MFM = MFM mode selected, opposite to MF mode.
                        HDS = head select
                        DS  = drive select
                        MT  = multi track operation
                        SK  = skip deleted data address mark

                   Command            # bytes    D7  6   5   4   3   2   1   0
                 read track              9       0  MFM  0   0   0   0   1   0
                                                 0   0   0   0   0 HDS DS1 DS0
                 specify                 3       0   0   0   0   0   0   1   1
                 sense drive status      2       0   0   0   0   0   1   0   0
                                                 0   0   0   0   0 HDS DS1 DS0
                 write data              9       MT MFM  0   0   0   1   0   1
                                                 0   0   0   0   0 HDS DS1 DS0
                 read data               9       MT MFM SK   0   0   1   1   0
                                                 0   0   0   0   0 HDS DS1 DS0
                 recalibrate             2       0   0   0   0   0   1   1   1
                                                 0   0   0   0   0   0 DS1 DS0
                 sense interrupt status 1        0   0   0   0   1   0   0   0
                 write deleted data      9       MT MFM  0   0   1   0   0   1
                                                 0   0   0   0   0 HDS DS1 DS0
                 read ID                 2       0  MFM  0   0   1   0   1   0
                                                 0   0   0   0   0 HDS DS1 DS0
                 read deleted data       9       MT MFM SK   0   1   1   0   0
                                                 0   0   0   0   0 HDS DS1 DS0
                 format track            10      0  MFM  0   0   1   1   0   1
                                                 0   0   0   0   0 HDS DS1 DS0
                 dumpreg **              1       0   0   0   0   1   1   1   0
                 seek                    3       0   0   0   0   1   1   1   1
                                                 0   0   0   0   0 HDS DS1 DS0
                 version **              1       0   0   0   1   0   0   0   0
                 scan equal *            9       MT MFM SK   1   0   0   0   1
                                                 0   0   0   0   0 HDS DS1 DS0
                 perpendicular mode **   2       0   0   0   1   0   0   1   0
                                                 0   0   0   0   0   0 WGATE GAP
                 configure **            4       0   0   0   1   0   0   1   1
                                                 0   0   0   0   0   0   0   0
                 verify                  9       MT MFM SK   1   0   1   1   0
                                                 EC  0   0   0   0 HDS DS1 DS0
                 scan low or equal *     9       MT MFM MK   1   1   0   0   1
                                                 0   0   0   0   0 HDS DS1 DS0
                 scan high or equal *    9       MT MFM MK   1   1   1   0   1
                                                 0   0   0   0   0 HDS DS1 DS0
                 relative seek **        3       1  DIR  0   0   1   1   1   1
                                                 0   0   0   0   0 HDS DS1 DS0

                 BEWARE: not every invalid command is treated as invalid!
                 *  Note: the scan commands aren't mentioned for the 82077AA.
                 ** Note: EHD controller commands.

03F6            reserved on FDC

03F6    r/w     FIXED disk controller data register
                 bit 7-4    reserved
                 bit 3 = 0  reduce write current
                         1  head select 3 enable
                 bit 2 = 1  disk reset enable
                         0  disk reset disable
                 bit 1 = 0  disk initialization enable
                         1  disk initialization disable
                 bit 0      reserved

03F7    r       diskette controller DIR (Digital Input Register, PC/AT mode)
                 bit 7 = 1 diskette change
                 bit 6-0   tri-state on FDC

                 bit 6     FIXED DISK write gate
                 bit 5     FIXED DISK head select 3 / reduced write current
                 bit 4     FIXED DISK head select 2
                 bit 3     FIXED DISK head select 1
                 bit 2     FIXED DISK head select 0
                 bit 1     FIXED DISK drive 1 select
                 bit 0     FIXED DISK drive 0 select

03F7    r       diskette controller DIR (Digital Input Register, PS/2 mode)
                 bit 7   = 1 diskette change
                 bit 6-3 = 1
                 bit 2       datarate select1
                 bit 1       datarate select0
                 bit 0   = 0 high density select (500Kb/s, 1Mb/s)

 conflicts with  bit 0     FIXED DISK drive 0 select

03F7    r       diskette controller DIR (Digital Input Register, PS/2 model 30)
                 bit 7   = 0 diskette change
                 bit 6-4 = 0
                 bit 3       -DMA gate from DOR register
                 bit 2       NOPREC from CCR register
                 bit 1       datarate select1
                 bit 0       datarate select0

03F7    w       configuration control register (PC/AT, PS/2)
                 bit 7-2      reserved, tri-state
                 bit 1-0 = 00  500 Kb/S mode
                         = 01  300 Kb/S mode
                         = 10  250 Kb/S mode
                         = 11  reserved

03F7    w       configuration control register (PS/2 model 30)
                 bit 7-3      reserved, tri-state
                 bit 2        NOPREC (has no function. set to 0 by hardreset)
                 bit 1-0 = 00  500 Kb/S mode
                         = 01  300 Kb/S mode
                         = 10  250 Kb/S mode
                         = 11  reserved
```

```
--------------------------------------------------------------------------------
03F8-03FF ----  serial port (8250,8251,16450,16550), same as 02E8,02F8 and 03E8

03F8    w       serial port, transmitter holding register, which contains the
                character to be sent. Bit 0 is sent first.
                 bit 7-0   data bits when DLAB=0 (Divisor Latch Access Bit)
        r       receiver buffer register, which contains the received character
                Bit 0 is received first
                 bit 7-0   data bits when DLAB=0 (Divisor Latch Access Bit)
        r/w     divisor latch low byte when DLAB=1

03F9    r/w     divisor latch high byte when DLAB=1
        r/w     interrupt enable register when DLAB=0
                 bits 7-4   reserved
                 bit 3 = 1  modem-status interrupt enable
                 bit 2 = 1  receiver-line-status interrupt enable
                 bit 1 = 1  transmitter-holding-register empty interrupt enable
                 bit 0 = 1  received-data-avail.int. enable (and 16550 timeout)

              - 16550 will interrupt if data exists in the FIFO and isn't read
                within the time it takes to receive four bytes or if no data is
                received within the time it takes to receive four bytes

03FA    r       interrupt identification register. Information about a pending
                interrupt is stored here. When the ID register is addressed,
                the highest priority interrupt is held, and no other interrupts
                are acknowledged until the CPU services that interrupt.
                 bit 7-6 = 00  reserved on 8250, 8251, 16450
                         = 11  if FIFO queues are enabled (16550 only)
                 bit 5-4 = 0 reserved
                 bit 3   = 0 reserved  8250, 16450
                         = 1 16550  timeout int. pending
                 bit 2-1 identify pending interrupt with the highest priority
                  = 11  receiver line status interrupt. priority=highest
                  = 10  received data available register interrupt. pr.=second
                  = 01  transmitter holding register empty interrupt. pr.=third
                  = 00  modem status interrupt. priority=fourth
                 bit 0 = 0  interrupt pending. contents of register can be used
                            as a pointer to the appropriate int.service routine
                         1  no interrupt pending

              - interrupt pending flag uses reverse logic, 0=pending, 1=none
              - interrupt will occur if any of the line status bits are set
              - THRE bit is set when THRE register is emptied into the TSR


03FA    w       16650 FCR  (FIFO Control Register)
                 bit 7-6 = 00  1 byte
                         = 01  4 bytes
                         = 10  8 bytes
                         = 11 14 bytes
                 bit 5-4 = 00 reserved
                 bit 3   = 1  change RXRDY  TXRDY pins from mode 0 to mode 1
                 bit 2   = 1  clear XMIT FIFO
                 bit 1   = 1  clear RCVR FIFO
```

```
              bit 0   = 1  enable clear XMIT and RCVR FIFO queues

           - bit 0 must be set in order to write to other FCR bits
           - bit 1 when set  the RCVR FIFO is cleared and this bit is reset
              the receiver shift register is not cleared
           - bit 2 when set  the XMIT FIFO is cleared and this bit is reset
              the transmit shift register is not cleared

03FB    r/w     line control register
              bit 7 = 1  divisor latch access bit (DLAB)
                      0  receiver buffer, transmitter holding, or interrupt
                         enable register access
              bit 6 = 1  set break enable. serial ouput is forced to spacing
                         state and remains there.
              bit 5 =    stick parity
              bit 4 = 1  even parity select
              bit 3 =    parity enable
                      1  even number of ones are sent and checked in the
                         data word bits and parity bit
                      0  odd number of ones are sent and checked
              bit 2 = 0  one stop bit
                      1  zero stop bit
              bit 1-0 00 word length is 5 bits
                      01 word length is 6 bits
                      10 word length is 7 bits
                      11 word length is 8 bits

03FC    r/w     modem control register
              bit 7-5 = 0  reserved
              bit 4 = 1  loopback mode for diagnostic testing of serial port
                         output of transmitter shift register is looped back
                         to receiver shift register input. In this mode
                         transmitted data is received immediately so that
                         the CPU can verify the transmit data/receive data
                         serial port paths.
              bit 3 = 1  auxiliary user-designated output 2
              bit 2 = 1  auxiliary user-designated output 1
              bit 1 = 1  force request-to-send active
              bit 0 = 1  force data-terminal-ready active

03FD    r       line status register
              bit 7 = 0  reserved
              bit 6 = 1  transmitter shift and holding registers empty
              bit 5 = 1  transmitter holding register empty. Controller is
                         ready toaccept a new character to send.
              bit 4 = 1  break interrupt. the received data input is held in
                         in the zero bit state longer than the time of start
                         bit + data bits + parity bit + stop bits.
              bit 3 = 1  framing error. the stop bit that follows the last
                         parity or data bit is a zero bit.
              bit 2 = 1  parity error. Character has wrong parity
              bit 1 = 1  overrun error. a character was sent to the receiver
                         buffer before the previous character in the buffer
                         could be read. This destroys the previous
                         character.
              bit 0 = 1  data ready. a complete incoming character has been
                         received and sent to the receiver buffer register.

03FE    r       modem status register
              bit 7 = 1  data carrier detect
              bit 6 = 1  ring indicator
              bit 5 = 1  data set ready
              bit 4 = 1  clear to send
              bit 3 = 1  delta data carrier detect
              bit 2 = 1  trailing edge ring indicator
              bit 1 = 1  delta data set ready
              bit 0 = 1  delta clear to send

           - bits 0-3 are reset when the CPU reads the MSR
           - bit 4 is the Modem Control Register RTS during loopback test
           - bit 5 is the Modem Control Register DTR during loopback test
           - bit 6 is the Modem Control Register OUT1 during loopback test
           - bit 7 is the Modem Control Register OUT2 during loopback test

03FF    r/w     scratch register
```

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- Richard W. Watson `<73042.1420@CompuServe.COM>`.
- Some of the information in this list was extracted from Frank van Gilluwe's *The Undocumented PC*, a must-have book for anyone programming down to the "bare metal" of a PC.
- Some of the information in this list from the shareware version of Dave Williams' DOSREF, v3.0.
- 8514/A hardware ports found in FractInt v18.0 source file FR8514A.ASM
- Compaq QVision info from the *COMPAQ QVision Graphics System Technical Reference Guide*, second edition (October 1993). Compaq part number 073A/0693.

Chapter 2

Data sheets

The following data sheets document the chips installed on Eos systems.

- i8259 Programmable Interrupt Controller
- NS16550 Unisersal Asynchronous Receiver/Transmitter with FIFOs
- i8253 Programmable Interval Timer
- DS12887 Real Timer Clock
- MC14469 Addressable Asynchronous Receiver/Transmitter (AART)